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EXAMINER	
THOMAS, SHANE M	
ART UNIT	PAPER NUMBER
2186	3

DATE MAILED: 08/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/702,202	KORGER, PETER	
	Examiner	Art Unit	
	Shane M Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *10 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

Figures 1a and 1b should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The figure 2 is objected to because output signals tag_valid[0] and tag_valid[N-1], output from flip-flop pair 48 and 46 respectively, are not visible. The labeling of the signals coincides with the hole-punch areas used to attach the drawings to the application file wrapper. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 10 is objected to because "FIFO locations" should be corrected to "FIFO location" (line 10) and "data have" should be corrected to "data has" (line 11) in order to maintain the tense of the claim.

Claim 18 is objected to because "storage locations is" of line 5 should be corrected to "storage *location* is" in order to reflect the correct plurality.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-15 and 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, line 2 is ambiguous and open to multiple interpretations. One interpretation is that the all of the storage locations compose a single memory element, *N* units (bits, bytes, etc.) wide, wherein *T*-bits of those *N* units are used for a tag. Another interpretation is an *N* number of memory "blocks," wherein each "block" is *X*-bits wide, with *T* of those bits tag bits. Yet another interpretation is an *N* number of memory "blocks," X-bits wide, with the memory *device* having *T* tag bits and not each of the memory "blocks." The examiner will examine the claim with respect to each memory "block" being a storage location and that each "block" having a number of bits, *T* of those bits being reserved for a tag.

Additionally, the phrase "*N*-bit read and write registers" of lines 3 and 5 are ambiguous and open to multiple interpretations. One such interpretation is that there are multiple "*N*-bit read" and "*N*-bit write registers" while another interpretation is that there exists a single *N*-bit read register and a single *N*-bit write register. Yet another interpretation is that there exists *N*-bit registers and based on the value of the register, suggests a read or a write. The examiner will examine the claim with respect to this latter interpretation with each *N* storage location having one of *N* read/write registers associated

with it. Applicant is reminded of 37 C.F.R. 1.75 (d)(1) which states that the claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description. (See 1.58(a).)

Further, lines 5-6 are ambiguous and open to multiple interpretations. The claim reads, "logic for comparing the contents of the read and write registers with corresponding contents of the storage locations...", thus indicating that only read and write registers corresponding to the same storage location will be compared. However lines 5-6 can also be interpreted to mean the logic is "comparing the content of the read and write registers *with* the content of the storage locations" in order to determine which of the storage locations have been written. In this case, the read and write registers are being compared to the values of the data in the storage locations. The examiner will examine the claim with regards to the logic comparing the contents of each read and write register that respectively correspond to the contents of one of the *N* storage locations.

Still further, on line 8, the term "status" is vague and thus open to multiple interpretations. The "status" of a "storage location" could indicate the "validity" of the location; it could indicate the location is pending for another device to access it or another of a plurality of interpretations.

Regarding claim 10, line 7, the term "status" is vague and thus open to multiple interpretations. The "status" of tag bits could indicate their validity; "status" could indicate tag bits are pending being written or another of a plurality of interpretations.

Regarding claim 11, the term "*N*-bit read and write registers" is ambiguous and open to multiple interpretations. One interpretation is that there is one and only one read and one and only one write register, each register *N* bits wide. This interpretation follows that the FIFO address of the location being written to or read from is "recorded" in the write or read register, respectively. Another interpretation is that there are *N* read and *N* write registers with each register 1 bit wide, and when an address in the FIFO is written to or read from, the corresponding write or read bit, respectively, is toggled. This "toggling" would "record" when the corresponding FIFO location is written to or read from.

Regarding claim 14, the phrase "suppress the logic level" is vague and open to multiple interpretations. One interpretation is that neither a logic low nor logic high is output, meaning a type of buffer is used and high impedance observed when the corresponding tag bits of a "FIFO location" are invalid. Another interpretation is that "suppressing the logic level" simply means that circuit logic will not consider the logic level of a signal because other logic in the circuit has "filtered" or "masked" the signal out and thus does not enable the invalid signal to effect future combinatorial logic. The examiner will refer to "suppressing the logic level" to be defined according to this latter example.

Regarding claims 17-20, lines 1, it is not clear if the term "indicator method" is the same as the "method for indicating status of a storage device" of claim 16, line 1, as "indicator method" lacks antecedent basis. Terminology within the claims must be consistent.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy (U.S. Patent No. 6,433,787) in view of applicant's admitted prior art.

Regarding claim 1, Murphy shows a memory system in figure 3 comprising a FIFO buffer 320 and a storage device 350, consisting of *N* storage locations, each storage location having a corresponding read/write flag bit 352. Since each entry contains a flag field, it can be seen that there are a total of *N* flag fields. When a corresponding read/write flag is valid (True) for the entry of the storage device 350 to be written to, the write logic 330 stalls until the flag is cleared by the read logic 360. When the write completes, the flag is set to True (see column 4, lines 16-19). Likewise, when an entry in the storage device is False, the read process stalls and waits for data to be written. After the location is marked valid by the write process, the data is then read out by the read logic and the flag bit is set to False (column 4, lines 24-26).

Murphy does not explicitly state that the data being read into the memory system 300 from bus 305 contains tag bits. Applicant's admitted prior art states on page 2, line 5, that "it is often advantageous to include tag bits along with the data when being written into a FIFO structure." One function of the prior art tags bits as admitted by the applicant is to assist in data transfers, since "less processing is required at the receiving end to

ascertain the nature of the transfer" (page 2, line 9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the storage device 350 of Murphy to incorporate tag bit storage locations. Doing so would have helped to alleviate some of the "overhead" bytes that contain addressing information usually sent with every pixel-byte over a graphic system bus (see column 1, line 62, thru column 2, line 5). This process would have further supported the "burst-transaction" mentioned by Murphy in column 2, lines 8-9; the tag bits could have been used for further aiding in specifying a chain of several related pixel-bytes to a destination, or used for verification purposes to have made sure the chain of pixel-bytes were sent to the correct area of the system that requested the pixels, after being read out of the memory device 300 of Murphy.

Regarding claim 2, the modified memory system 300 of Murphy does not explicitly state that data is written to and read out of the system using different clock cycles. However as is known in the art, and admitted by the applicant on page 1, line 25, FIFO systems often employ different clocks for reading and writing data. The dual-clock system is especially useful for "burst mode" data transfers (line 26). One embodiment of the memory system of Murphy is for use in a graphics system with pixel data being transferred through the system. Murphy's modified memory system would have been useful in the video camera example presented by the applicant in line 27. It would have been obvious to one in the art at the time the invention was made to utilize the memory system of Murphy in the video camera system in order for pixel data to be written into the memory system by the camera, and then read out by a slower clock of another system, such as a computer as admitted by the applicant on page 2, line 1.

Regarding claim 3, Murphy states that for a read operation to occur from a storage location from storage device 350, the read logic 360 must wait until write logic 330 sets the read/write flag bit 352 of the corresponding storage location to be read to True (column 4, lines 19-26). Therefore, it can be seen that combinatorial logic must be constantly checking to determine which storage locations have been written to and not read. The process of ANDing the read/write flag bit with a logic 1 mask would have been one design of this implementation.

Regarding claim 5, the examiner will refer to storage locations of storage device 350 that have been written to but not read (read/write bit 352 is True) as "valid" storage locations.

Claims 6-8, 10,16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy (U.S. Patent No. 6,433,787) in view of applicant's admitted prior art in further view of Zaidi et al (U. S. Patent No. 6,574,689).

Regarding claims 6 and 7, the modified memory system 300 of Murphy lacks a way to compare valid tag bits across every storage location of storage device 350. As was stated by the applicant, the tag bits of a system could be used to denote the particular I/O device a packet of data originated from. Further the applicant states that this tag system is beneficial in that it would be possible to determine whether the FIFO contained data from a specific I/O device without have to read each entry in the queue (page 7, lines 14-19). Using the case of a particular I/O device (e.g. videocamera of the above mentioned example) sending data packets to the graphic system (figure 6) of Murphy, the graphics system may want or require information regarding which pixels, corresponding to different I/O devices, are in the memory system 300. One reason for

this need could be to store the expectant data into a buffer dedicated to a particular I/O device (see applicant's admitted prior art page 7, lines 17-19). Thus it would have been useful to determine the tag information of the "valid" storage locations. Only tag bits corresponding to the "valid" locations would be useful since the data associated with the "invalid" locations would have either been previously read out or not yet written into the storage device 350 by the write logic.

Zaidi shows in figure 2 that an AND gate 212 can be used to transfer tag information from a queue 200. The "tag" bit in figure 2 is being used as a valid bit and is ANDed with a logic mask 214. As is known in the art, the mask is used to determine if in fact the tag bit is valid by ANDing it with a logic 1. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the memory system of Murphy to have included the AND gates used by Zaidi to determine the validity of tag bits in each storage location. Instead of a valid entry mask 214 being used by Murphy (as the other input into the tag bit AND gate) to determine a valid tag bit of a storage location, the read/write flag bit 352 of the corresponding storage location would have been used since the read/write flag would have been a logic 1 if and only if the storage location was "valid" (data in the storage location had not yet been read out). Since *N* storage locations comprise storage device 350, *N* AND gates would have been used for *each* tag bit because it would have been necessary to analyze the tag bits of each storage location when determining which tag bits are "valid" tag bits (i.e. corresponding to "valid" storage locations).

Regarding claim 8, now that every tag bit of every storage location has been determined to be "valid" or not, Murphy does not have logic to further determine which

tag bits are "valid" *across* the storage device. The applicant's admitted prior art, figure 1b, and page 7, lines 11-14, state that a series of OR gates can be used to simultaneously determine if the logic level of any of the tag bits are "valid." Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the memory system of Murphy to have utilized OR gates connected to the output of the tag bits' AND gates in order to determine which, if any, of the tag bits are active or "valid" in the memory system. Referring to the previous example stated above of the graphic system of Murphy utilizing tag bits to identify the I/O device a data packet corresponding to a particular location of the storage device had originated from, it would have been seen that the output of the OR gates would have effectively determined which device (based on the tag bits) from which data residing in the valid locations of the storage device had originated from.

Regarding claim 10, the examiner is referring to the storage device 350 (which includes flag bits 352) as a "first-in-first-out" (FIFO) system. This is validated since for a system writing data to memory system 300 with consecutive offset addresses, no reordering would be needed. Therefore the first data segment read into the memory system 300 will be the first segment *written* to the "FIFO" storage system 350 (from buffer 320) and thus the first segment *read* out of the "FIFO" storage system will be that same data segment.

Regarding claim 10, the same rejections as claims 1, 2, and 8 are applied. Claim 1's rejection is applied to line 3; claim 2's rejection is applied to lines 4-6; and claim 8's rejection is applied to lines 7-8. Claim 8's rejection shows how every tag bit of the storage device 350 of Murphy would have been ANDed with the corresponding

read/write flag bit 352 to determine which tag bits correspond to a valid storage location (location that has been written to but no read from). The examiner is regarding the validity or invalidity of the tag bits as the "status" of the tag bits.

Regarding claim 16, the same rejections for claims 1, 2, 3, 5-8 are applied. Claim 1's rejection is applied to line 3; claim 2's rejection is applied to lines 4-6; and claims 3's rejection is applied to lines 8-9 (lines 1-2, page 15 of the application). Claim 3, and 5-7's rejections are applied to line 9 because the examiner is defining "detecting active tag bits" as using combinatorial logic to only compare tags bits of "valid" storage locations. Claim 8's rejection is applied to lines 11-12 since a logic signal is generated from the output of the OR gates corresponding to each tag bit in the "FIFO."

Regarding claim 19, the same rejection as claim 8 is applied.

Claims 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of applicant's admitted prior art in further view of Zaidi in further view of Klingelhofer (U.S. Patent 5,884,099). Since reading and writing can occur at synchronous intervals, but not necessarily synchronous with each other, it would have been beneficial to synchronize the output of the ORed valid tag signals so that the read logic of Murphy (360 figure 3) could have gathered the "status" of the tag bits corresponding to data that had been written but not read out and had this information available for the read logic at the same time the read logic had determined what location to read out. Non-synchronous behavior between the valid tag signals and the read logic could have resulted in the read logic losing "valid" tag information since the result of the combinatorial logic may have come after the read logic begin accessing a storage location was read out. As stated above, this tag information could have been used to send specific

data to a buffer dedicated to a specific I/O device (applicant's admitted prior art, page 7, line 18). Figure 1 of Klingelhofer shows synchronization circuitry 136 and teaches that this circuitry adjusts the output of the FIFO flag circuitry to be synchronous with the output clock 116 to enable output from the FIFO (column 3, lines 61-63). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Murphy to include the output synchronization of Klingelhofer so that the read circuitry would have been synchronous with the output of the valid tag OR gates. This crucial modification would have been able to overcome the aforementioned problem of losing valid tag data. With Klingelhofer's teaching, the read logic would clock in the tag bit information when the combinatorial logic had produced a valid calculation for the tag bits of the storage system.

Allowable Subject Matter

Claims 4,11-15, 17, and 18, would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 4, Murphy in view of the applicants admitted prior art does not teach an XOR associated with each N storage location comparing the *i*th bit of the write register with the *i*th bit of the read register.

Regarding claims 11-15, Murphy in view of the applicants admitted prior art in further view of Zaidi in further view of Klingelhofer does not teach two distinct read and

write registers corresponding to each FIFO location comprising combinatorial logic between the two registers to compare their contents in order to determine which locations on the FIFO have been written and not read.

Regarding claims 17 and 18, Murphy in view of the applicants admitted prior art in further view of Zaidi in further view of Klingelhofer does not teach an indicator method for a storage device that associates a storage location flag in a first register and a second register, toggling the respective read or write register when data is written to the corresponding storage location, and comparing the contents of the flags of corresponding storage locations to determine if the location has been written to and not read. Further it does not teach ANDing the result of the flag comparison with the logic state of the tags bits in the corresponding storage location.

Conclusion

Prior art made of record and not relied upon is considered pertinent to applicant's disclosure in PTO-892. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (703) 605-0725. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 764-7239 for regular communications and (703) 764-7239 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Shane M. Thomas
August 5, 2003

DAVID L. ROBERTSON
PRIMARY EXAMINER